Lecture 090 – Large Signal MOSFET Model

LECTURE 090 – LARGE SIGNAL MOSFET MODEL
LECTURE ORGANIZATION

Outline
• Introduction to modeling
• Operation of the MOS transistor
• Simple large signal model (SAH model)
• Subthreshold model
• Short channel, strong inversion model
• Summary

CMOS Analog Circuit Design, 2nd Edition Reference
Pages 73-78 and 97-99

INTRODUCTION TO MODELING

Models Suitable for Understanding Analog Design
The model required for analog design with CMOS technology is one that leads to understanding and insight as distinguished from accuracy.

This lecture is devoted to the simple model suitable for design not using simulation.
### Categorization of Electrical Models

<table>
<thead>
<tr>
<th>Linearity</th>
<th>Time Dependence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear</td>
<td>Small-signal, midband $R_{in}$, $A_v$, $R_{out}$ ($\cdot$TF)</td>
</tr>
<tr>
<td>Nonlinear</td>
<td>DC operating point $i_D = f(v_D, v_G, v_S, v_B)$ ($\cdot$OP)</td>
</tr>
</tbody>
</table>

Based on the simulation capabilities of SPICE.

---

**OPERATION OF THE MOS TRANSISTOR**

**Formation of the Channel for an Enhancement MOS Transistor**

- **Subthreshold** ($V_G < V_T$)
  - $V_B = 0$
  - $V_S = 0$
  - $V_G < V_T$
  - $V_D = 0$

- **Threshold** ($V_G = V_T$)
  - $V_B = 0$
  - $V_S = 0$
  - $V_G = V_T$
  - $V_D = 0$

- **Strong Threshold** ($V_G > V_T$)
  - $V_B = 0$
  - $V_S = 0$
  - $V_G > V_T$
  - $V_D = 0$
Transconductance Characteristics of an Enhancement NMOSFET when $V_{DS} = 0.1V$

Output Characteristics of the Enhancement NMOS Transistor for $V_{GS} = 2V_T$
Output Characteristics of the Enhanced NMOS when $v_{DS} = 2V_T$

Further increase in $V_G$ will cause the FET to become active.

SPICE Input File:

```
Output Characteristics for NMOS
M1 6 1 0 0 MOS1 w=5u l=1.0u
VGS1 1 0 1.0
M2 6 2 0 0 MOS1 w=5u l=1.0u
VGS2 2 0 1.5
M3 6 3 0 0 MOS1 w=5u l=1.0u
VGS3 3 0 2.0
M4 6 4 0 0 MOS1 w=5u l=1.0u
VGS4 4 0 2.5

M5 6 5 0 0 MOS1 w=5u l=1.0u
VGS5 5 0 3.0
VDS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u +gamma=0.4 +lambda=.04 phi=.7)
dc vds 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4), ID(M5)
.end
```

CMOS Analog Circuit Design © P.E. Allen - 2010
Transconductance Characteristics of an Enhancement NMOS Transistor

SPICE Input File:

```
Transconductance Characteristics for NMOS
M1 1 6 0 0 MOS1 w=5u l=1.0u
VDS1 1 0 1.0
M2 2 6 0 0 MOS1 w=5u l=1.0u
VDS2 2 0 2.0
M3 3 6 0 0 MOS1 w=5u l=1.0u
VDS3 3 0 3.0
M4 4 6 0 0 MOS1 w=5u l=1.0u
VDS4 4 0 4.0
M5 5 6 0 0 MOS1 w=5u l=1.0u
VDS5 5 0 5.0
VGS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u +gamma=0.4 lambda=.04 phi=.7)
.dc vgs 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4), ID(M5)
.probe
.end
```

Fig. 3.1-7

SIMPLE LARGE SIGNAL MODEL (SAH MODEL)

**Large Signal Model Derivation**

1.) Let the charge per unit area in the channel inversion layer be

\[
Q(y) = -C_{ox}[v_{GS} - v(y) - V_T] \quad \text{(coul./cm²)}
\]

2.) Define sheet conductivity of the inversion layer per square as

\[
\sigma_S = \mu_o Q(y) \frac{\text{cm}^2}{\text{v·s} \cdot \text{coulombs} \cdot \text{cm}^2} = \text{amps/volt} = \frac{1}{\Omega/\text{sq}}.
\]

3.) Ohm's Law for current in a sheet is

\[
J_S = \frac{i_D}{W} = -\sigma_S E_y = -\sigma_S \frac{dv}{dy} \quad \rightarrow \quad dv = \frac{-i_D}{\sigma_S W} \quad dy = \frac{-i_D dy}{\mu_o Q(y) W} \quad \rightarrow \quad i_D dy = -W \mu_o Q(y) dv
\]

4.) Integrating along the channel for 0 to \(L\) gives

\[
\int_{0}^{V_{DS}} i_D dy = - \int_{0}^{V_{DS}} W \mu_o Q(y) dv = \int_{0}^{V_{DS}} W \mu_o C_{ox} [v_{GS} - v(y) - V_T] dv
\]

5.) Evaluating the limits gives

\[
i_D = \frac{W \mu_o C_{ox}}{L} \left[(v_{GS} - V_T) v(y) - \frac{v^2(y)}{2}\right]_0^{V_{DS}} \rightarrow \quad i_D = \frac{W \mu_o C_{ox}}{L} \left[(v_{GS} - V_T) v_{DS} - \frac{V_{DS}^2}{2}\right]
\]
**Saturation Voltage - \( V_{DS(sat)} \)**

Interpretation of the large signal model:

The saturation voltage for MOSFETs is the value of drain-source voltage at the peak of the inverted parabolas.

\[
\frac{di_D}{dv_{DS}} = \frac{\mu_o C_{ox} W}{L} \left[ (v_{GS} - V_T) - v_{DS} \right] = 0
\]

\[v_{DS(sat)} = v_{GS} - V_T\]

Useful definitions:

\[
\frac{\mu_o C_{ox} W}{L} = \frac{K'W}{L} = \beta
\]

---

**The Simple Large Signal MOSFET Model**

Regions of Operation of the MOS Transistor:

1.) Cutoff Region:

\( v_{GS} - V_T < 0 \)

\( i_D = 0 \)

(Ignores subthreshold currents)

2.) Active Region

\[ 0 < v_{DS} < v_{GS} - V_T \]

\[ i_D = \frac{\mu_o C_{ox} W}{2L} [2(v_{GS} - V_T) - v_{DS}] v_{DS} \]

3.) Saturation Region

\[ 0 < v_{GS} - V_T < v_{DS} \]

\[ i_D = \frac{\mu_o C_{ox} W}{2L} (v_{GS} - V_T)^2 \]

---

**Output Characteristics of the MOSFET:**
Illustration of the Need to Account for the Influence of $v_{DS}$ on the Simple Sah Model

Compare the Simple Sah model to SPICE level 2:

\[ K' = 44.8 \mu A/V^2 \]
\[ k = 0, \quad v_{DS}(sat) = 1.0\text{V} \]
\[ K' = 29.6 \mu A/V^2 \]
\[ k = 0, \quad v_{DS}(sat) = 1.0\text{V} \]
\[ K' = 44.8 \mu A/V^2 \]
\[ k = 0.5, \quad v_{DS}(sat) = 1.0\text{V} \]

$V_{GS} = 2.0\text{V}$, $W/L = 100\mu m/100\mu m$, and no mobility effects.

Modification of the Previous Model to Include the Effects of $v_{DS}$ on $V_T$

From the previous derivation:

\[
\int_{0}^{L} i_D \, dy = - \int_{0}^{v_{DS}} \frac{v_{DS}}{W \mu_o Q(y)} \, dv = \int_{0}^{v_{DS}} \frac{v_{DS}}{W \mu_o C_{ox}} [v_{GS} - v(y) - V_T] \, dv
\]

Assume that the threshold voltage varies across the channel in the following way:

$V_T(y) = V_T + kv(y)$

where $V_T$ is the value of $V_T$ the at the source end of the channel and $k$ is a constant.

Integrating the above gives,

\[
i_D = \frac{W \mu_o C_{ox}}{L} \left[ (v_{GS} - V_T) v(y) - (1+k) \frac{v^2(y)v_{DS}}{2} \right]_{0}^{v_{DS}}
\]

or

\[
i_D = \frac{W \mu_o C_{ox}}{L} \left[ (v_{GS} - V_T)v_{DS} - (1+k) \frac{v_{DS}^2}{2} \right]
\]

To find $v_{DS}(sat)$, set the $di_D/dv_{DS}$ equal to zero and solve for $v_{DS} = v_{DS}(sat)$,

\[
v_{DS}(sat) = \frac{v_{GS} - V_T}{1 + k}
\]

Therefore, in the saturation region, the drain current is

\[
i_D = \frac{W \mu_o C_{ox}}{2(1+k)L} (v_{GS} - V_T)^2
\]

For $k = 0.5$ and $K' = 44.8 \mu A/V^2$, excellent correlation is achieved with SPICE 2
Influence of $v_{DS}$ on the Output Characteristics

Channel modulation effect:

As the value of $v_{DS}$ increases, the effective $L$ decreases causing the current to increase.

Illustration:

Note that $L_{eff} = L - X_d$

Therefore the model in saturation becomes,

$$i_D = \frac{K'W}{2L_{eff}}(v_{GS} - V_T)^2 \quad \Rightarrow \quad \frac{di_D}{dv_{DS}} = -\frac{K'W}{2L_{eff}}(v_{GS} - V_T)^2 \quad \Rightarrow \quad \frac{dL_{eff}}{dv_{DS}} = \frac{i_D}{L_{eff}} \frac{dX_d}{dv_{DS}} = \lambda i_D$$

Therefore, a good approximation to the influence of $v_{DS}$ on $i_D$ is

$$i_D \approx i_D(\lambda = 0) + \frac{di_D}{dv_{DS}} v_{DS} = i_D(\lambda = 0)(1 + \lambda v_{DS}) = \frac{K'W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

Channel Length Modulation Parameter, $\lambda$

Assume the MOS is transistor is saturated-

$$\therefore \quad i_D = \frac{\mu C_{ox}W}{2L} (v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

Define $i_D(0) = i_D$ when $v_{DS} = 0V$.

$$\therefore \quad i_D(0) = \frac{\mu C_{ox}W}{2L} (v_{GS} - V_T)^2$$

Now,

$$i_D = i_D(0)[1 + \lambda v_{DS}] = i_D(0) + \lambda i_D(0) v_{DS}$$

Matching with $y = mx + b$ gives the value of $\lambda$
Influence of Channel Length on $\lambda$

Note that the value of $\lambda$ varies with channel length, $L$. The data below is from a 0.25$\mu$m CMOS technology.

![Graph showing Channel Length Modulation vs Channel Length for NMOS and PMOS](image)

Most analog designers stay away from minimum channel length to get better gains and matching at the sacrifice of speed.

Influence of the Bulk Voltage on the Large Signal MOSFET Model

The components of the threshold voltage are:

\[ V_T = \text{Gate-bulk work function (} \phi_{MS} \text{)} + \text{voltage to change the surface potential (-2} \phi_F \text{)} + \text{voltage to offset the channel-bulk depletion charge (-} Q_b/C_{ox} \text{)} + \text{voltage to compensate the undesired interface charge (-} Q_{ss}/C_{ox} \text{)} \]

We know that

\[ Q_b = \gamma \sqrt{2\phi F1 + |v_{BS}|} \]

Therefore, as the bulk becomes more reverse biased with respect to the source, the threshold voltage must increase to offset the increased channel-bulk depletion charge.
Influence of the Bulk Voltage on the Large Signal MOSFET Model - Continued

Bulk-Source ($v_{BS}$) influence on the transconductance characteristics-

In general, the simple model incorporates the bulk effect into $V_T$ by the previously developed relationship:

$$V_T(v_{BS}) = V_{T0} + \gamma \sqrt{2|\phi_f| + |v_{BS}|} - \gamma \sqrt{2|\phi_f|}$$

Summary of the Simple Large Signal MOSFET Model

N-channel reference convention:

Non-saturation-

$$i_D = \frac{W\mu_o C_{OX}}{L} \left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right] (1 + \lambda v_{DS})$$

Saturation-

$$i_D = \frac{W\mu_o C_{OX}}{L} \left[(v_{GS}-V_T)v_{DS(sat)} - \frac{v_{DS(sat)}^2}{2}\right] (1 + \lambda v_{DS}) = \frac{W\mu_o C_{OX}}{2L} \left[(v_{GS}-V_T)^2(1 + \lambda v_{DS})\right]$$

where:

- $\mu_o = $ zero field mobility (cm$^2$/volt·sec)
- $C_{OX} = $ gate oxide capacitance per unit area (F/cm$^2$)
- $\lambda = $ channel-length modulation parameter (volts$^{-1}$)
- $V_T = V_{T0} + \gamma \sqrt{\sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|}}$
- $V_{T0} = $ zero bias threshold voltage
- $\gamma = $ bulk threshold parameter (volts$^{-0.5}$)
- $2|\phi_f| = $ strong inversion surface potential (volts)

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert the current.
**Silicon Constants**

<table>
<thead>
<tr>
<th>Constant Symbol</th>
<th>Constant Description</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_G$</td>
<td>Silicon bandgap (27°C)</td>
<td>1.205</td>
<td>V</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann’s constant</td>
<td>1.381x10^{-23}</td>
<td>J/K</td>
</tr>
<tr>
<td>$n_i$</td>
<td>Intrinsic carrier concentration (27°C)</td>
<td>1.45x10^{10}</td>
<td>cm^{-3}</td>
</tr>
<tr>
<td>$\varepsilon_o$</td>
<td>Permittivity of free space</td>
<td>8.854x10^{-14}</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\varepsilon_{si}$</td>
<td>Permittivity of silicon</td>
<td>11.7 $\varepsilon_o$</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\varepsilon_{ox}$</td>
<td>Permittivity of SiO$_2$</td>
<td>3.9 $\varepsilon_o$</td>
<td>F/cm</td>
</tr>
</tbody>
</table>

**MOSFET Parameters**

Model Parameters for a Typical CMOS Bulk Process (0.25μm CMOS n-well):

<table>
<thead>
<tr>
<th>Parameter Symbol</th>
<th>Parameter Description</th>
<th>Typical Parameter Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{T0}$</td>
<td>Threshold Voltage ((V_{BS} = 0))</td>
<td>(0.5 \pm 0.15) (-0.5 \pm 0.15)</td>
<td>V</td>
</tr>
<tr>
<td>$K'$</td>
<td>Transconductance Parameter (in saturation)</td>
<td>(120.0 \pm 10%) (25.0 \pm 10%)</td>
<td>μA/V^2</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>Bulk threshold parameter</td>
<td>(0.4) (0.6)</td>
<td>((V)^{1/2})</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Channel length modulation parameter</td>
<td>(0.32 \ L=L_{min}) (0.06 \ L \geq 2L_{min}) (0.56 \ L=L_{min}) (0.08 \ L \geq 2L_{min})</td>
<td>((V)^{-1})</td>
</tr>
<tr>
<td>$2\mid\phi F\mid$</td>
<td>Surface potential at strong inversion</td>
<td>(0.7) (0.8)</td>
<td>V</td>
</tr>
</tbody>
</table>
**SUBTHRESHOLD MODEL**

**Large-Signal Model for Weak Inversion**

The electrons in the substrate at the source side can be expressed as,

\[ n_p(0) = n_{po} \exp\left(\frac{\phi_s}{V_t}\right) \]

The electrons in the substrate at the drain side can be expressed as,

\[ n_p(L) = n_{po} \exp\left(\frac{\phi_s - V_{DS}}{V_t}\right) \]

Therefore, the drain current due to diffusion is,

\[ i_D = qAD_n \left(\frac{n_p(L) - n_p(0)}{L}\right) = \frac{W}{L} qXn_p \exp\left(\frac{\phi_s}{V_t}\right) \left[ 1 - \exp\left(-\frac{V_{DS}}{V_t}\right) \right] \]

where \( X \) is the thickness of the region in which \( i_D \) flows.

In weak inversion, the changes in the surface potential, \( \Delta \phi_s \), are controlled by changes in the gate-source voltage, \( \Delta v_{GS} \), through a voltage divider consisting of \( C_{ox} \) and \( C_{js} \), the depletion region capacitance.

\[ \frac{d\phi_s}{dv_{GS}} = \frac{C_{ox}}{C_{ox} + C_{js}} = \frac{1}{n} \rightarrow \phi_s = \frac{v_{GS}}{n} + k_1 = \frac{v_{GS} - V_T}{n} + k_2 \]

where

\[ k_2 = k_1 + \frac{V_T}{n} \]

Define \( I_t \) as

\[ I_t = qXn_p \exp\left(\frac{k_2}{V_t}\right) \]

to get,

\[ i_D = \frac{W}{L} I_t \exp\left(\frac{v_{GS} - V_T}{nV_t}\right) \left[ 1 - \exp\left(-\frac{V_{DS}}{V_t}\right) \right] \]

where \( n = 1.5 - 3 \)

If \( V_{DS} > 0 \), then

\[ i_D = I_t \exp\left(\frac{v_{GS} - V_T}{nV_t}\right) \left[ 1 + \frac{V_{DS}}{V_A}\right] \]

The boundary between nonsaturated and saturated is found as,

\[ V_{ov} = V_{DS(sat)} = V_{ON} = V_{GS} - V_T = 2nV_t \]
SHORT CHANNEL, STRONG INVERSION MODEL

What is Velocity Saturation?

The most important short-channel effect in MOSFETs is the velocity saturation of carriers in the channel. A plot of electron drift velocity versus electric field is shown below.

An expression for the electron drift velocity as a function of the electric field is,

\[ v_d \approx \frac{\mu_n E}{1 + E/E_c} \]

where

- \( v_d \) = electron drift velocity (m/s)
- \( \mu_n \) = low-field mobility (≈ 0.07 m^2/V·s)
- \( E_c \) = critical electrical field at which velocity saturation occurs

**Short-Channel Model Derivation**

As before,

\[ J_D = J_S = \frac{i_D}{W} = Q_i(y) v_d(y) \rightarrow i_D = W Q_i(y) v_d(y) = \frac{W Q_i(y) \mu_n E}{1 + E/E_c} \rightarrow i_D \left[ 1 + \frac{E}{E_c} \right] = W Q_i(y) \mu_n E \]

Replacing \( E \) by \( dv/dy \) gives,

\[ i_D \left[ 1 + \frac{1}{E_c} \frac{dv}{dy} \right] = W Q_i(y) \mu_n \frac{dv}{dy} \]

Integrating along the channel gives,

\[ \int_0^L i_D \left[ 1 + \frac{1}{E_c} \frac{dv}{dy} \right] dy = \int_0^{v_{DS}} W Q_i(y) \mu_n dv \]

The result of this integration is,

\[ i_D = \frac{\mu_n C_{ox}}{2 \left( 1 + \frac{v_{DS}}{E_c} \right) L} \left[ 2 (v_{GS} - V_T) v_{DS} - v_{DS}^2 \right] = \frac{\mu_n C_{ox}}{2 \left( 1 + \theta v_{DS} \right) L} \left[ 2 (v_{GS} - V_T) v_{DS} - v_{DS}^2 \right] \]

where \( \theta = 1/(E_c L) \) with dimensions of V·s. 
**Saturation Voltage**

Differentiating $i_D$ with respect to $v_{DS}$ and setting equal to zero gives,

$$V'_{DS}(sat) = \frac{1}{\theta} \sqrt{1 + \frac{2\theta(V_{GS} - V_T)}{V_{GS} - V_T}} = (V_{GS} - V_T) \left( 1 - \frac{\theta(V_{GS} - V_T)}{2} + \cdots \right)$$

if

$$\frac{\theta(V_{GS} - V_T)}{2} < 1$$

Therefore,

$$V'_{DS}(sat) = V_{DS}(sat) \left( 1 - \frac{\theta(V_{GS} - V_T)}{2} + \cdots \right)$$

Note that the transistor will enter the saturation region for $v_{DS} < v_{GS} - V_T$ in the presence of velocity saturation.

---

**Large Signal Model for the Saturation Region**

Assuming that

$$\frac{\theta(V_{GS} - V_T)}{2} < 1$$

gives

$$V'_{DS}(sat) = (V_{GS} - V_T)$$

Therefore the large signal model in the saturation region becomes,

$$i_D = \frac{K'}{2[1 + \theta(V_{GS} - V_T)]} \frac{W}{L} (v_{GS} - V_T)^2, \quad v_{DS} \geq (V_{GS} - V_T) \left( 1 - \frac{\theta(V_{GS} - V_T)}{2} + \cdots \right)$$
The Influence of Velocity Saturation on the Transconductance Characteristics

The following plot was made for $K' = 110 \mu A/V^2$ and $W/L = 1$:

![Plot showing the influence of velocity saturation on transconductance characteristics.](image)

Note as the velocity saturation effect becomes stronger, that the drain current-gate voltage relationship becomes linear.

Circuit Model for Velocity Saturation

A simple circuit model to include the influence of velocity saturation is shown:

We know that

$$i_D = \frac{K'W}{2L} (v_{GS'} - V_T)^2 \quad \text{and} \quad v_{GS} = v_{GS'} + i_D R_{SX}$$

or

$$v_{GS'} = v_{GS} - i_D R_{XS}$$

Substituting $v_{GS'}$ into the current relationship gives,

$$i_D = \frac{K'W}{2L} (v_{GS} - i_D R_{SX} - V_T)^2$$

Solving for $i_D$ results in,

$$i_D = \frac{K'}{2[1 + K'\frac{W}{L} R_{SX}(v_{GS} - V_T)^2]} \sqrt[\theta L]{\frac{W}{L} (v_{GS} - V_T)^2}$$

Comparing with the previous result, we see that

$$\theta = K' \frac{W}{L} R_{SX} \quad \Rightarrow \quad R_{SX} = \frac{\theta L}{K'W} = \frac{1}{E_c K'W}$$

Therefore for $K' = 110 \mu A/V^2$, $W = 1 \mu m$ and $E_c = 1.5 \times 10^6 V/m$, we get $R_{SX} = 6.06 k\Omega$. 
SUMMARY

• The modeling of this lecture is devoted to understanding how the circuit works
• The two primary current-voltage characteristics of the MOSFET are the transconductance characteristic and the output characteristic
• The simple Sah large signal model is good enough for most applications and technology
• The Sah model can be improved in the region of the knee and for the weak dependence of drain current on drain-source voltage in the saturation region
• Most designers do not work at minimum channel length because of the channel length modulation effect and because worse matching occurs for small areas
• The threshold voltage is increased as the bulk-source is reverse biased
• The subthreshold model accounts for very small currents that flow in the channel when the gate-source voltage is smaller than the threshold voltage
• The subthreshold current is exponentially related to the gate-source voltage
• Velocity saturation occurs at minimum channel length and can be modeled by including a source degeneration resistor with the simple large signal model